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### **A New Model of Step Recovery Diode for CAD**

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#### **ABSTRACT**

**A** new step recovery diode (SRD) model for CAD is developed by considering the voltage ranip in the SRD and using a DC measurement to extract a model parameter. This model can be directly used in commercial circuit simulators for designs of SRD circuits. Examples of using this model to analyse a comb generator and a frequency multiplier are given.

#### **I. Introduction**

Step recovery diodes (SRDs) are strongly nonlinear devices, which are used extensively in comb generators, frequency multipliers, and wave formers 111. **As** a frequency multiplier the **SRD** is used for example in millimeter wave link radios.

The design of SRD circuits is mainly based 011 an idealized diode model consisting of two linear circuits  $[2]$ . However, designs based on this model have very limited accuracy, and high performances of actual circuits are usually achieved by experimental adjustments. Thus, simulation and optimization of SRD circuits by computers are desirable to accomplish more accurate circuit designs.

However, such an idealized model can not be directly used in commercial circuit simulators, since the circuit-solving algorithms used by simulators are based on algorithms like the Newton-Raphson algorithm. Therefore, constitutive relationships of the device must be differentiable with respect to voltage and current and these derivatives with respect to voltage and current should be continuous, too

In 1983, a computer simulation model was

proposed by Goldman [3]. That model was established on the base of the model of a conventional p-n junction diode and characterized by experiments. However, as we know, an SRD is essentially different from a conventional p-n junction diode, and therefore, its characteristics cannot be modeled very well by this method under all design conditions.

In this paper a model of the SRD is developed for the *CAD* of SRD circuits. It can be used in circuit simulators, e.g *"HP* Microwave and **RF** Design Systems" and **"APLAC"** [4]. First, a modified basic model of the **SRD** is established, using a DC measurement to extract a model parameter. Then a continuous model is developed by considering the voltage ramp in the SRD. Finally, applications of this model to analyses of comb generators and frequency multipliers are given.

#### **II. Modified SRD basic model**

An ideal step recovery diode functions as a switch from a high impedance state to a low impedance state, corresponding to a small reverse bias capacitor **(C,)** and an infinite forward bias capacitor  $(C_f)$ . However, there should be a finite **C,** for a more realistic modeling of the **SKD** The corresponding charge-voltage curve is illustrated in Fig.l, and the relationship can be written as follows:

ws:  
\n
$$
Q(V) = \begin{cases} C_f (V - V_0) & V \ge V_0 \\ C_f (V - V_0) & V < V_0 \end{cases}
$$
\n(1)

where  $v_e = \phi$ , which is the contact potential of the diode.

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**CH 1577-4/95/0000-1459\$01** *.OO 0* **<sup>1995</sup>IEEE.** *1995* **IEEE MTT-S Digest** 

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In addition to the two constant capacitors, I he series parasitic resistance, the package inductance and capacitance should be taken into consideration The equivalent circuit of an **SRD**  Including all these factors is shown in [Fig.](#page-3-0) **2** C, is a small constant capacitance equal to the junction capacitance given by the manufacturer; whereas  $C_f$ inust be characterized using DC measurements as follows:

When the **SRD** is forward biased, the p-n junction acts like a dynamic or nonlinear resistor  $(R_f)$ . The relationship of  $C_f$ ,  $R_f$  and the minority carrier lifetime can be related as given by Kotzebue *[5]* ,

$$
\tau = R_f C_f
$$

where  $\tau$  is the minority carrier lifetime of the SRD given by the manufacturer. Through **DC** measurements we can obtain the **I-V** characteristic of the **SRD** under test **A** typical I-V curve of the **SRD**  *(HP-0835)* is shown in [Fig.](#page-3-0) **3.** It can be seen that the forward biased resistance turns into a very small and nearly constant resistance right after the diode is forward biased. In the case of the diode under test, the value of the forward biased resistance is of the order of 0.1 ohm, which corresponds to a forward biased capacitance of 10 *1tF.* 

#### **III. New Model**

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However, due to the discontinuity of the first differential of Q with respect to V at  $V=v_0$ , the simulator may have trouble in converging. This discontinuity cannot describe accurately the real physical phenomena occurring in a real SRD, either. Therefore, a more complex continuous model is required

The limiting factor in switching from  $C_f$  to  $C_r$  is the rapidity with which charge can be extracted from the i layer. **A** ramp in voltage is formed when the stored free charge carrier density at the p<sup>+</sup>-i or i-n<sup>+</sup> boundary vanishes.

A continuous model to describe the voltage ramp was proposed by Moll and Hamilton *[6].*  The voltage drop across the diode and the stored charge in *I* layer during the process when the

voltage ramp is formed can be related by the following equation,

$$
V = \frac{T_R}{\mathbf{e} \mathbf{v} \mathbf{A}} \left[ \frac{W^2}{4} - W \sqrt{\frac{2D}{T_R}} \sqrt{Q} + \frac{2D}{T_R} Q \right].
$$
 (2)

Here v, **A** and D are the average velocity of carriers in the space charge limit range, the working area of the diode and the ambipolar diffision constant, respectively.

Assuming that the ramping begins at  $Q_R$ , a fraction of the total stored charge Q, and that  $Q_R$ corresponds to a small field free width  $W_f$  in the i layer, where

$$
W_{ff} = \left(\frac{8DQ}{I_R}\right)^{\frac{1}{2}} \qquad (3)
$$

then eq. (2) is approximated as follows,

$$
V = \frac{T_R}{\epsilon v A} \left( \frac{w^2}{4} - W \sqrt{Q} \sqrt{\frac{2Q}{T_R}} \right) \tag{4}
$$

Therefore, **an** SRD can be modeled so that at large forward voltages it is equivalent to a forward bias capacitor  $C_f$  corresponding to the conducting state, and that the voltage ramp begins when the forward bias is reduced to the contact potential  $\phi$ . After that there is a fast transition and finally a rounding off until all the stored charge has been swept out from the *i* layer. Then the nonconducting state continues as the voltage becomes further negative. Thus, the conducting state is continuously transformed to the nonconducting state through a process of turn-off

Accordingly, the voltage and the stored charge are related by piecewise curves as shown in Fig. **4.** Straight lines BC and **A0** represent the conducting and nonconducting bias capacitances, respectively. The BO section is a parabolic curve representing the turn-off process. The continuity condition requires that at the beginning of the ramping, i.e. at point B, the stored charge *Q* and its first derivatives with respect to V are continuous. The same requirement is applied at the end of'

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the turn-off, i.e. at point 0. Thus, the piecewise relationship of Q and V can be defined as follows:

$$
Q = \begin{cases} C_r V & V \le 0 \\ C (V+a)^2 - b & 0 < V < \Phi \\ C_r V + Q_{rmp} - C_r \Phi & V \ge 0. \end{cases}
$$
 (5)

where  $Q_{mm}$  is the stored charge at the beginning of ramping. This parameter and the parameters a, b, and c can be determined by the boundary conditions as follows

$$
Q=Q_{rmp}
$$
 and  $dQ/dV=C_f$ , when  $V = \phi$ ,  
  $Q=0$ , and  $dQ/dV=C_r$ , when  $V = 0$ .

Applying these boundary conditions, we obtain,

$$
C_{r}V \qquad \qquad V \leq 0
$$

$$
Q = \begin{cases}\n\frac{C_f - C_r}{2\phi} \left( V + \frac{C_r \Phi}{C_f - C_r} \right)^2 - \frac{C_r^2}{2 (C_f - C_r)} \phi & 0 < V < \Phi \\
C_f V - \frac{C_f - C_r}{2} \phi & V \ge \Phi.\n\end{cases}
$$
\n(6) [5]

#### **IV. Applications**

Using this new model, we have simulated comb-generators and frequency multipliers. The package parasitic inductance of 1 **nH** and capacitance of 0.2 pF are included in this model of *HP-*0835 diode. A L-section input matching network is designed for both the comb generator and the frequency multiplier. *An* open shunt stub low pass filter and a shunt shorted stub band pass filter are designed for input and output circuits of the multiplier, respectively. [Fig. 5](#page-3-0) shows the transient analysis results of a comb generator. [Fig. 6](#page-3-0) shows the simulation circuit of a frequency multiplier. [Fig. 7](#page-3-0) shows the harmonic balance analysis results of a  $10\times$  frequency multiplier with input frequency of 1.333 *GHz* and input power level of 19 dBm.

#### **V. References**

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 $Fig. 1.$  Modified Characteristic of the SRD.

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Fig. 5. simulation of a comb generator. From top down: input voltage, diode current, output voltage.



Fig. 3. Input impedance vs.  $C_f$ 



Fig. 4. Modified characteristic of the SRD considering voltage ramp.

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Fig. 6. Simulation circuit of a frequency multiplier.



Fig. 7. Simulation of a frequency multiplier. (Symbols refer to Fig. 6.)

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